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test circuits connected between said input terminals and said output terminals via test signal transmission paths, wherein at least part of said first bus lines or said second bus lines is shared by said test signal transmission paths, and wherein the test circuit is activated in a test mode and is deactivated in a normal operation mode.

REMARKS

The Office Action dated November 21, 2002, has been received and carefully noted. The period for response having been extended from February 21, 2003 to March 21, 2003, by the attached Petition for Extension of Time, the amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 11-14, 18-21, 26-29 and 30 have been amended. No new matter has been added by the amendment made herein. Accordingly, claims 1-48 are pending in the present application, and are respectfully submitted for reconsideration.

As a preliminary matter, Applicant acknowledges the Examiner's withdrawal of the Restriction Requirement presented in the previous action dated August 22, 2002, and therefore, all claims 1-48 are currently pending in the present application.

Claims 12-14 and 19-21 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The Office Action took the position that some of the limitations recited in claims 12-14 and 19-21 contradict with independent claims 11 and 18, respectively. Applicant submits that the amendments made to claims 12-14 and 19-21 correct the deficiencies noted in the Office Action and place these claims in compliance with U.S. Patent practice.

Claims 18-21, 24-26, 28, 30 and 31 were rejected under 35 U.S.C. § 102(b) as being anticipated by JP-05053857 A (hereinafter "JP '857"). Applicant respectfully submits that each of claims 18-21, 24-26, 28, 30 and 31 recites subject matter that is neither disclosed nor suggested in this cited prior art.

Claim 18 recites an electronic device having first and second semiconductor devices connected to each other with a plurality of bus lines. The first semiconductor device includes a first output circuit connected to one of the bus lines for supplying the bus line with a first logical output signal, an inversion output circuit connected to the bus line for supplying the bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the first logical output signal, and a comparison circuit connected to the bus line. The second semiconductor device includes an input circuit connected to the bus line for acquiring a first bus line signal, and a second output circuit connected to the input circuit for supplying a corresponding bus line with the first bus line signal. The comparison circuit receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

Claim 24 recites a first semiconductor device that judges a connection between the first semiconductor device and a second semiconductor device connected thereto with bus lines. The first semiconductor device includes an output circuit connected to each bus line that supplies each bus line with a first logical output signal. The second semiconductor device receives a first bus line signal and supplies a bus line with a

second logical output signal being an inverted signal of the first bus line signal. The first semiconductor device also includes a comparison circuit connected to each bus line that receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the connection between the first semiconductor device and the second semiconductor device.

Claim 25 recites a first semiconductor device that judges a connection between the first semiconductor device and a second semiconductor device connected thereto with bus lines. The first semiconductor device includes an output circuit connected to each bus line that supplies each bus line with a first logical output signal. The second semiconductor device receives a first bus line signal. The first semiconductor device also includes an inversion output circuit connected to each bus line that supplies each bus line with a second logical output signal being an inverted signal of the first logical output signal after the output circuit supplying the first logical output signal, and a comparison circuit connected to each bus line that receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the connection between the first semiconductor device and the second semiconductor device.

Claim 30 recites the semiconductor device having input terminals, output terminals, an internal circuit, first bus lines that connect to input terminals and the internal circuit, respectively, and second bus lines that connect the output terminals and the internal circuit, respectively. In addition, the semiconductor device includes test circuits connected between the input terminals and the output terminals via test signal

transmission paths. At least a part of the first bus lines or the second bus lines is shared by the test signal transmission paths, and wherein the test circuit is activated in a test mode and is deactivated in a normal operation mode.

Accordingly, the present invention provides a test circuit for detecting a short circuit failure or open circuit failure of bus lines connecting plural semiconductor devices incorporated in an electronic device. Therefore, the present invention results in the advantage where the circuit area for testing is decreased, which increases efficiency.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the presently pending claims, and therefore fails to provide the advantages which are provided by the present invention.

JP '857 discloses a circuit for testing connection between LSI. The circuit is equipped with a test data register 2 to invert a signal between LSIs from an LSI-B 20 and to store the signal in an LSI-A10, a comparison register 4 to store the inverted output of this test data register 2, a comparator 5 to compare the contents of the test data 2 with the contents of the comparison register 4, and loops 1, 3, 6 and 7 to transmit the LSI-A10 and the LSI-B20 and to return the data to the original test data register 2 after inverting them while being equipped with the test data register 2. When both lines 103 and 104 are exchanging LSI signals are correctly connected, a coincident output '0' and of the comparator 5 is compressed to a line 109 and when one of the lines 103 and 104 is not connected at least, a comparative non-coincident output '1' is outputted to a line 107.

Applicant respectfully submits that each and every element recited within claims 18, 24, 25 and 30 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicant respectfully submits that the test method and test circuit for an electronic device as recited in the present application is clearly distinct from that which is illustrated in JP '857. Specifically, it is respectfully submitted that JP '857 fails to disclose or suggest the limitation of a second semiconductor device inverting a first logical output signal and provides the first semiconductor device with an inverted signal (second logical output signal), and also fails to disclose or suggest the limitation of a test circuit that is activated in a test mode and is deactivated in a normal operation mode.

As mentioned abovem JP '857 merely shows a first logical output signal is provided from a register (2) of a first semiconductor device (10) to a second semiconductor device (20), and a second logical output signal is fed back from the second semiconductor device to the first semiconductor device without inverting the second logical output signal. A comparator (5) in the first semiconductor device (10) compares a test data signal (first logical signal; 107) which is output from the register (2), and an inverted signal (108), which is generated by inverting the test signal (second logic signal; 104) fed back from the second semiconductor device (20) using two inverters (1, 3) in the first semiconductor device (10). In contrast, the present invention provides a second semiconductor device which inverts a first logical output signal and provides a first semiconductor device with an inverted signal (second logical output signal). By using the inverted signal of the present invention, residual charges are

generated on a bus line when the bus line is opened, and therefore a determination error of connection is avoided.

As for claim 30, Applicant submits that JP '857 merely discloses selectors (6, 7), each of which selects test data or normal operation data in response to a test mode signal. However, the cited reference does not disclose a test circuit that is activated in a test mode and is deactivated in a normal operation mode. By deactivating the test circuit in a normal operation mode as provided in the present invention, it is possible to provide an internal circuit with a signal or output a signal from the internal circuit via first bus lines or second bus lines at least a part of which is shared as test signal transmission paths. Furthermore, by sharing the bus lines also provided in the present invention, the circuit area is avoided from increasing.

In view of the above, Applicant respectfully submits that JP '857 fails to disclose or suggest each and every element recited within claims 18, 24, 25 and 30.

Claim 28 has been amended to depend from independent claim 18. Accordingly, as for claim 19-21, 28, and 31, Applicant submits that each of these claims recites subject matter which is neither disclosed nor suggested by the cited prior art. In particular, each of these claims depend on claims 18 and 30, respectively, and therefore, incorporates each and every limitation recited within claims 18 and 30, respectively, therein. Accordingly, Applicant submits that each of claims 19-21, 28 and 31 also recites subject matter which is neither disclosed or suggested by JP '857 for at least the reasons set forth above with respect to claims 18 and 30.

As for the rejection of claim 26, it is noted claim 26 has been amended to depend from independent claim 11. Accordingly, the rejection with respect to claim 26 shall be addressed below.

Claims 1-17, 22, 23, 27, 29 and 32-48 were rejected under 35 U.S.C. § 103(a) as being unpatentable over JP '857. In making this rejection, the Office Action took the position that JP '857 disclosed all of the elements of the claimed invention with the exception of showing the subject matter as noted in the Office Action. The Office Action noted that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify JP '857 to achieve the claimed invention. Applicant respectfully traverses this rejection. Applicant submits that each of claims 1-17, 22, 23, 27, 29 and 32-48 recite subject matter that is neither disclosed nor suggested in the cited prior art.

Claim 1 recites a method of testing an electronic device including first and second semiconductor devices connected to each other with a plurality of bus lines. The method includes the step of having the first semiconductor device supplying a selected one of the bus lines with a first logical output signal, and having the second semiconductor device acquiring a first bus line signal from the selected bus line. In addition, the steps include having the second semiconductor device invert the first bus line signal to generate a second logical output signal and transmitting the second logical output signal to the first semiconductor. The first semiconductor device receives a second bus line signal from the selected bus line, and the first semiconductor device compares the first logical output signal and the second bus line signal to judge a

connection between the first semiconductor device and the second semiconductor device.

Claim 6 recites a method of testing an electronic device including first and second semiconductor devices connected to each other with a plurality of bus lines. The method comprises the steps of having the first semiconductor device apply a selected one of the bus lines with a first logical output signal, and having the second semiconductor device acquire a first bus line signal from the selected bus signal. After outputting the first logical output signal, the first semiconductor device generates a second logical output signal being an inverted signal of the first logical output signal and supplying the selected bus line with a second logical output signal. The second semiconductor device outputs the acquired first bus line signal; the first semiconductor device receives a second bus line signal from the selected bus line. The first semiconductor device further compares the first logical output signal and the received second bus line signal to judge a connection between the first semiconductor device and the second semiconductor device.

Claim 11 recites an electronic device having a first and second semiconductor devices connected to each other with a plurality of bus lines. The first semiconductor device includes a first output circuit connected to one of the bus lines for supplying the bus line with a first logical output signal, and a comparison circuit connected to the bus line. The second semiconductor device includes an input circuit connected to the bus line for acquiring a first bus line signal, and a second output circuit connected to the input circuit for inverting the first bus line signal to generate a second logical output

signal, and supplying a corresponding bus line with the second logical output signal. The comparison circuit receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

Claim 47 recites a semiconductor device having input terminals, output terminals, an internal circuit, and test circuits connected between the input terminals and the output terminals. Furthermore, the semiconductor device includes clamp circuits connected to the input terminals that clamp the respective input terminals to a specific potential in a test mode, and release the clamp at the input terminals in a normal operation mode.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicant's invention as set forth in claims 1-17, 22, 23, 27, 29 and 32-48, and therefore fails to provide the advantages that are provided by the present invention.

Applicant respectfully submits that each and every element recited within claims 1, 6, 11 and 47 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicant respectfully submits that the test method and test circuit for an electronic device as recited in the present application is clearly distinct from that which is illustrated in JP '857. Specifically, it is respectfully submitted that JP '857 fails to disclose or suggest the limitation of a second semiconductor device inverting a first logical output signal and provides the first semiconductor device with an

inverted signal (second logical output signal), and fails to disclose or suggest the limitation of a clamp circuit that clamps respective input terminals to a specific potential.

As for claims 1, 6 and 11, JP '857 merely discloses a first logical output signal is provided from a register (2) of a first semiconductor device (10) to a second semiconductor device (20), and a second logical output signal is fed back from the second semiconductor device to the first semiconductor device without inverting the second logical output signal. A comparator (5) in the first semiconductor device (10) compares a test data signal (first logical signal; 107) which is output from the register (2), and an inverted signal (108), which is generated by inverting the test signal (second logic signal; 104) fed back from the second semiconductor device (20) using two inverters (1, 3) in the first semiconductor device (10). However, it is submitted that the cited reference does not disclose that the second semiconductor device inverts a first logical output signal and provides the first semiconductor device with an inverted signal (second logical output signal). By using the inverted signal as provided by the present invention, residual charges are generated on a bus line when the bus line is opened, and therefore a determination error of connection is avoided. Accordingly, JP '857 fails to obtain such an advantage of the present invention.

As for claim 47, it is submitted that JP '857 fails to disclose or suggest a clamp circuit that clamps respective input terminals to a specific potential. By using the clamp circuit as provided by the present invention, an error operation of a test circuit is avoided when a bus line is opened. As such, the cited reference cannot obtain such an advantage of the present invention.

In view of the above, Applicant respectfully submits that JP '857 fails to disclose or suggest each and every element recited within claims 1, 6, 11 and 47. In addition, Applicant submits that it would not have been obvious to one of ordinary skilled in the art to modify the cited prior art to yield the present invention.

As for the rejection of claim 26, it is noted claim 26 has been amended to depend from independent claim 11. Accordingly, as for claims 2-5, 7-10, 12-17, 22, 23, 26, 27, 29, 32-46 and 48, Applicant submits that each of these claims cite subject matter which is neither disclosed nor suggested by the cited prior art. In particular, each of claims 2-5, 7-10, 12-17, 22, 23, 26, 27, 29, 32-46 and 48 depends on claims 1, 6, 11, 18 and 30, respectively. Therefore, each of these claims incorporates each and every limitation recited within independent claims 1, 6, 11, 18 and 30, respectively therein. Therefore, Applicant submits that each of claims 2-5, 7-10, 12-17, 22, 23, 26, 27, 29, 32-46 and 48 also recite subject matter which is neither disclosed nor suggested by JP '857 for at least the reasons set forth above with respect to claims 1, 6, 11, 18 and 30.

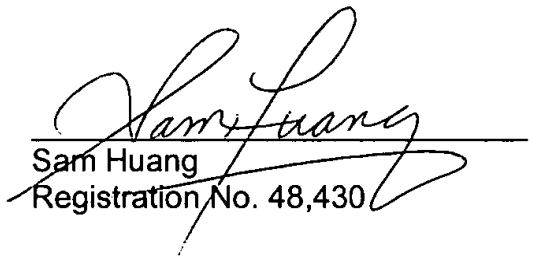
In view of the above, Applicant respectfully submits that claims 1-48, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art ,and therefore respectfully requests that claims 1-48 be found allowable and that this application be passed to issue.

If for any reasons, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact by

telephone the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to Attorney Docket number 108075-09034.

Respectfully submitted,



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Enclosures: Marked-Up Copy of Amended Claims
Petition for Extension of Time (one month)

MARKED-UP COPY OF AMENDED CLAIMS

11. (Once Amended) An electronic device comprising first and second semiconductor devices connected to each other with a plurality of bus lines, wherein the first semiconductor device includes:

a first output circuit connected to [each] one of the bus [line] lines for supplying [each] the bus line with a first logical output signal, and

a comparison circuit connected to [each] the bus line; and

the second semiconductor device includes:

an input circuit connected to [each] the bus line for acquiring a first bus line signal, and

a second output circuit connected to the input circuit for inverting the first bus line signal to generate a second logical output signal, and supplying a corresponding bus line with the second logical output signal, wherein the comparison circuit receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a [judgement] judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

12. (Once Amended) The electronic device of claim 11, wherein the semiconductor device includes a plurality of first output circuits and one of the bus lines is a selected bus line, and the first output circuit corresponding to [a] the selected bus line supplies the selected bus line with the first logical output signal having a first logical value, and the other first output circuits corresponding to the other bus lines supplies the other bus lines with signals having a second logical value.

13. (Once Amended) The electronic device of claim 11, wherein the first semiconductor device includes a plurality of first output circuits and at least one bus line is adjacent to another bus line, and [the] a first output circuit corresponding to [a first] the at least one bus line [adjacent to the second bus line] supplies the first bus line with the first logical output signal having a first logical value, and [the] a first output circuit corresponding to the [second] another bus line supplies the [second] another bus line with a signal having a second logical value.

14. (Once Amended) The electronic device of claim 11, wherein the first semiconductor device includes a first group of first output circuits corresponding to a first group of the bus lines adjacent to the second group of the bus lines and a second group of the first output circuits corresponding to the second group of the bus lines, wherein the first group supplies the first group of the bus lines with the first logical output signals each having a first logical value, and [a] the second group [of the first output circuits corresponding to the second group of the bus lines] supplies the second group of the bus lines with signals each having a second logical value.

18. (Once Amended) An electronic device comprising first and second semiconductor devices connected to each other with a plurality of bus lines, wherein the first semiconductor device includes:

a first output circuit connected to [each] one of the bus [line] lines for supplying [each] the bus line with a first logical output signal,

an inversion output circuit connected to [each] the bus lines for supplying [each] the bus line with a second logical output signal being an inverted signal of the first

logical output signal after the first output circuit supplies the first logical output signal, and

a comparison circuit connected to [each] the bus line; and

the second semiconductor device includes:

an input circuit connected to [each] the bus line for acquiring a first bus line signal, and

a second output circuit connected to the input circuit for supplying a corresponding bus line with the first bus line signal, wherein the comparison circuit receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a [judgement] judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

19. (Once Amended) The electronic device of claim 18, wherein the first semiconductor device includes a plurality of first output circuits and one of the bus lines is a selected bus line, and the first output circuit corresponding to [a] the selected bus line supplies the selected bus line with the first logical output signal having a first logical value, and the other first output circuits corresponding to non-selected bus lines supply the non-selected bus lines with signals each having a second logical value.

20. (Once Amended) The electronic device of claim 18, wherein the first semiconductor device includes a plurality of first output circuits and at least one bus line is adjacent to another bus line, and the first output circuit corresponding to [a first] the at least one bus line [adjacent to a second bus line] supplies the [first] at least one bus line

with the first logical output signal having a first logical value, and the first output signal corresponding to the [second] another bus line supplies the [second] another bus line with a signal having a second logical value.

21. (Once Amended) The electronic device of claim 18, wherein the first semiconductor device includes a first group of the first output circuits corresponding to a first group of the bus lines adjacent to a second group of the bus lines and a seond group of the first output circuits corresponding to the second group of the bus lines, and wherein the first group supplies the first group of the bus lines with the first logical output signals each having a first logical value, and the second group [of the first output circuits corresponding to the second group of the bus lines] supplies the second group of the bus lines with signals each having a second logical value.

26. (Once Amended) [A measured semiconductor] The electronic device [connected to a measuring semiconductor device with bus lines, comprising] of claim 11, wherein:

the input circuit comprises a larch circuit that receives a logical signal supplied from the measuring semiconductor device via one of the bus lines, and

the second output circuit comprises a logical circuit connected to the latch circuit that inverts the latched logical signal to generate an inverted logical signal.

27. (Once Amended) The [measured semiconductor] electronic device of claim 26, [wherein the measured semiconductor device] further [comprises] comprising a reset circuit connected to the latch circuit, that resets the latch circuit in response to either the first logical output signal or a command signal on the bus line.

28. (Once Amended) [A measured semiconductor] An electronic device [connected to a measuring semiconductor device with bus lines, comprising] of claim 18, wherein:

the input circuit comprises a latch circuit [that receives a logical signal supplied from the measuring semiconductor device through a bus line], and

the second output circuit comprises a logical circuit connected to the latch circuit[, that outputs the latched logical signal].

29. (Once Amended) The [measured semiconductor] electronic device of claim 28, [wherein the measured semiconductor device] further [comprises] comprising a reset circuit connected to the latch circuit, that resets the latch circuit in response to either the first logical output signal or a command signal on the bus line.

30. (Once Amended) A semiconductor device comprising:

input terminals,

output terminals,

an internal circuit,

first bus lines that connect the input terminals and the internal circuit, respectively,

second bus lines that connect the output terminals and the internal circuit, respectively, and

test circuits connected between said input terminals and said output terminals via test signal transmission paths, wherein at least part of said first bus lines or said second

bus lines is shared by said test signal transmission paths, and wherein the test circuit is activated in a test mode and is deactivated in a normal operation mode.